**National University of Computer and Emerging Sciences**

**(Islamabad Campus)**

Department of Computer Science

EE-109 Digital Logic Design (DLD)

Final Exam (Summer 2013)

**Instructor :** Mr. Jawad Hassan

Thursday, 1st August 2013

**Total Marks: 145 Time Allowed: 3 hour**

1. **Attempt on the Question Paper in the given space. NO EXTRA SHEET will be provided/accepted.**
2. After asked to commence the exam, please verify that you have **15** **different printed pages** including this title page.
3. There are **4 questions**. Attempt all of them. It is advisable to go through the paper once before starting with the first question.
4. Exam is closed books, closed notes. Please see that the area in your threshold is clean. You will be charged for any material which can be classified as ‘helping in the paper’ found near you.
5. **Calculator is not allowed.**
6. Students who attempt the paper with lead pencils loose the right to get them rechecked.
7. **The invigilator present is not supposed to answer any questions. No one may come to your room for corrections and you are not supposed to request to call anyone. Make assumptions wherever required and clearly mark them.**

**Note: Clearly and completely label all the diagrams**

**Roll No: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Question** | **1** | **2** | **3** | **4** | **Total** |
| Points | 35 | 35 | 40 | 35 | **145** |
| Score |  |  |  |  |  |

Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question # 1[3 + 3 + 6 + 8 + 8 +7 = 35]**

1. Reduce the following expression to three literals. [3]

**X'Z' + XYZ + XZ'**

1. Convert (445.625)10 to binary and then convert the resulting binary number to octal and hexadecimal. Show your method. [3]
2. Using two (2 x 4) decoders, enable and external gates design a combinational circuit defined by following two functions. [6]
3. F1(x,y,z) = (y’ + z)x’
4. F2(x,y,z) = ∑(0,1,4,5)
5. Implement following function with a 4x1 and 2x1 multiplexers. [8]

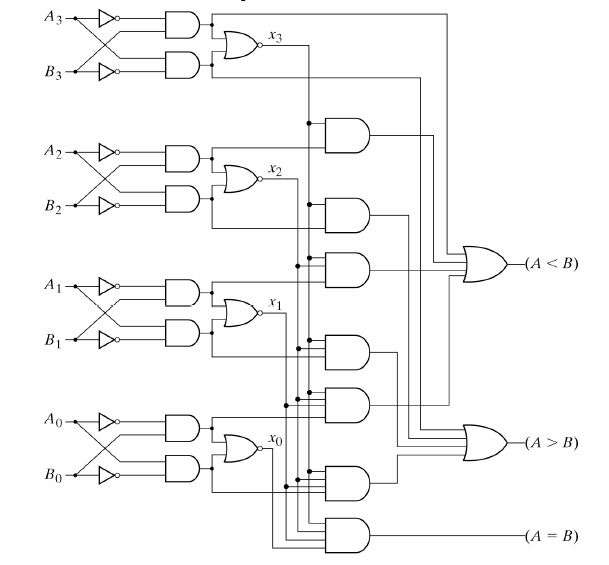
F(A,B,C,D) = ∑(0,2,3,6,9,12,14,15)

1. A 4-bit magnitude comparator circuit is shown below: [8]

Give the expression for F(A<B). Label the output of all gates when comparing two numbers

A = 1100

B = 1010



1. Define Pi and Gi for the Carry look-ahead adder than give the expression for all the four carry stages (Ci). [7]

**Question # 2[4 + 9 + 10 + 12 = 35]**

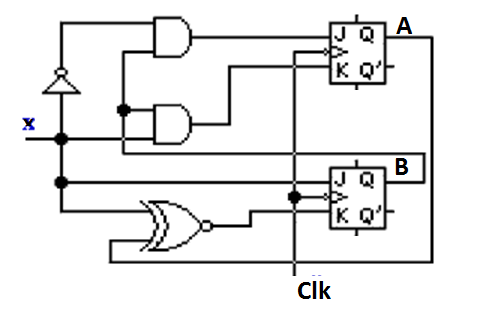
1. Draw and label the circuit diagram of a positive edge triggered D-flip flop in master slave configuration using two D latch blocks. [4]
2. A sequential circuit with two D flip flops, A and B; two inputs, x and y; and one output z, is specified by the following next state and output equations:

A (t+1) = x’y + xA’

B (t+1) = xB + y’A

z = B+x’y

1. Draw the logic diagram of the circuit. [3]
2. List the state table for the sequential circuit. [3]
3. Draw the corresponding state diagram. [3]
4. Analyze the following circuit with JK flip flops and provide the flip flop input equations, state table and state diagram. [10]



1. Design a sequential circuit using T flip-flop by using following State transition diagram. Treat unused states as don’t cares. [12]



**Question # 3[10 + 12 + 8 + 10 = 40]**

1. Design a two-bit counter using JK flip-flops which has one input x. [10]

When x=0, the counting sequence is 11, 01, 00, 10 and repeats.

When x=1, the counting sequence is 01, 11, 10, 00 and repeats.

1. Design a 4 bit Modulo-9 counter (i.e. the counter goes up till 8 only and then goes back to 0). Clearly show all the design steps. Use only T-flip flops. Only diagrams as solution to this question are not acceptable. [12]

**Note**: Treat unused states as don’t cares.

1. Draw and label the circuit diagram of a universal shift register using four 4 x 1 multiplexers and four D flip flops. The shift register should operate according to the following table. [8]

|  |  |  |
| --- | --- | --- |
| **S1** | **S0** | **Operation** |
| 0 | 0 | Reset to 0 |
| 0 | 1 | Shift left |
| 1 | 0 | Parallel Load |
| 1 | 1 | Complement the input |

1. Students of Batch BSCS-2012 have developed a new flip-flop named LM Flip-Flop. When inputs of L and M are 00, 01, 10 and 11, the flip-flop is cleared to zero, complements, sets to 1, and no change occurs respectively. For LM Flip-Flop: [10]
   1. Tabulate its characteristic table
   2. Tabulate excitation table
   3. Derive its excitation table
   4. Construct D-type Flip-Flop using LM flip-flop.

**Question # 4[13 + 12 + 10 = 36]**

1. Implement the following functions using a PLA. Draw and label the PLA diagram clearly showing all the connections. [13]
   1. F1 (w,x,y,z) = Σ (1,4,5,6,9,15)
   2. F2 (w,x,y,z) = Σ (1,5,6,9,11,12,13)
   3. F3 (w,x,y,z) = Σ (1,2,4,5,10,12,13,14,15)
   4. F4 (w,x,y,z) = Σ (2,4,6,7,10,11,14,15)
2. Implement the following functions using the PAL. [12]

F1 = ABC’ +B’CD’

F2 = A + BD

F3 = A’B + CD + B’D’

F4 = ABC’ + CD’ + AC’D’ + A’B’C’D

1. Implement following functions using the ROM. Give the ROM table and Draw the circuit. [10]

F1 (A,B,C,D) = A’BC + C’D + AD

F2 (A,B,C,D) = AB + CD + AC’D’

F3 (A,B,C,D) = B’D + ACD

F4 (A,B,C,D) = AD + BCD + A’B’